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 For: STATUS INDICATORS FOR FLASH MEMORY

(Title)

Enclosed are:

- ☒ Seveteen (17) sheet(s) of Drawings.
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Basic Fee:			
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x 11	\$
x 40	\$
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Respectfully submitted,

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UNITED STATES PATENT APPLICATION
FOR
STATUS INDICATORS FOR FLASH MEMORY

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STATUS INDICATORS FOR FLASH MEMORY

FIELD OF THE INVENTION

The present invention relates to the field of semiconductor memories. More particularly, the present invention relates to providing a programming suspend status signal and a protection status signal for a nonvolatile memory.

BACKGROUND OF THE INVENTION

Status registers are often used to store status information relating to the internal operations of a semiconductor integrated circuit ("IC"). Memory ICs or devices, such as flash electrically erasable programmable read only memory ("EEPROM") devices, may store information in a status register to indicate whether an operation (e.g., an erase operation, a programming operation, a read operation, etc.) is in progress or is completed. The status register may also indicate whether a specific operation has been completed successfully or unsuccessfully. Such information often provides necessary or desirable information to other components in a system.

For example, the processor or CPU in a system may need to know when an erase operation performed on a memory device (such as a flash memory device) is completed before requesting the memory device to perform a programming operation. Additionally, the processor in a system may want to know whether an erase operation to a specific memory location has been suspended. Typically, an erase operation takes a much longer time to complete as compared to a programming or read operation. For example, an erase operation may take a few milliseconds ("ms"), whereas a programming operation may take 7-8 microseconds (" μ s") and a reading operation may take 85 nanoseconds ("ns"). Thus, when an erase operation to a specific memory location is suspended, the processor may program or read data from a different memory location rather than waiting for the completion

of the current erase operation. The ability to suspend an erase operation may improve the overall performance of a flash memory device.

Typically, a status register stores multiple memory bits in which one or more of the memory bits may be used to provide a specific status signal. The status signal may be sent as an output from the memory device via a designated output pin when polled or via the data input/output ("I/O") pins of a memory device in response to a read status register command.

Figure 1 illustrates one embodiment of a status register for a prior art flash memory device that is capable of performing programming, erase, and read operations. The status register 100 includes the five memory locations 101 through 105 with each memory location storing at least one memory bit. For the embodiment shown in Figure 5, the status register 100 provides five status signals. The memory location 101 stores Vpp status ("VPPS") information; the memory location 102 stores byte write and set lock bit status ("BWSLBS") information; the memory location 103 stores erase and clear lock bits status ("ECLBS") information; the memory location 104 stores erase suspend status ("ESS") information; and the memory location 105 stores write state machine status ("WSMS") information.

The VPPS information indicates whether Vpp, the programming voltage, is at an acceptable voltage level or not at an acceptable voltage level. If Vpp is not at an acceptable voltage level, then the current operation may be aborted. The BWSLBS information indicates an unsuccessful byte write operation or a successful byte write operation. Alternatively, the BWSLBS information indicates an unsuccessful set master/block lock bit operation or a successful set master/block lock bit operation. The ECLBS information indicates an unsuccessful block erasure operation or a successful block erasure operation. Alternatively, the ECLBS information indicates an unsuccessful

clear lock bits operation or a successful clear lock bits operation. The ESS information indicates that the block erase operation is suspended or that the block erase operation is in progress/completed. The WSMS information indicates that the write state machine is ready or is busy.

5 The VPPS signal, the BWSLBS signal, the ECLBS signal, the ESS signal, and the WSMS signal are provided are outputted in response to a read status register command. Furthermore, the WSMS signal is outputted by polling a dedicated status output pin (e.g., pin).

10 The prior art memory device described above did not, however, provide the feature of suspending a programming operation. Therefore, a programming operation specifying a particular memory location could not be suspended in order to perform another operation, such as a read operation to another memory location, while the programming operation is suspended. In certain situations, it may be more efficient to perform a read operation
15 (which requires less time than a write operation) while a programming operation is suspended, rather than waiting until the programming operation is completed.

20 Additionally, the prior art memory device described above did not provide the feature of indicating whether an unsuccessful program or erase operation was due to an attempt to access data in a protected memory block. A prior art protection mechanism was implemented by the setting and clearing of memory bits (i.e., lock bits) that correspond to the various memory blocks in the memory device. The lock bits are stored in a miniature array referred to as the block lock mini-array. The lock bits within the block lock
25 mini-array are set to indicate that the corresponding memory block is locked, and cleared (or not set) to indicate that the corresponding memory block is unlocked. A read, program, or erase operation may be performed on any

unlocked memory block. A program or erase operation may not, however, be performed on any locked memory block unless an override lock operation is first performed on the locked memory block.

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SUMMARY OF THE INVENTION

A memory device is described that has a control circuit coupled to a memory array and a register. The register is configured to store at least one bit indicating the suspend status of a write operation. The control circuit is
5 configured to update the register and to control the output of a status signal representing the suspend status of the write operation.

A memory device is described that has a control circuit coupled to a memory array and a register. The register is configured to store at least one bit indicating the protection status of a data modification operation. The control
10 circuit is configured to update the register and to control the output of a status signal representing the protection status of the data modification operation.

A method is also described for providing the suspend status of a programming operation in a memory device. A programming operation to a memory location is performed. Prior to the completion of the programming
15 operation, a suspend status signal is received. It is determined whether or not to suspend the programming operation. If the programming operation is suspended, a status register is updated, if necessary, to indicate the programming operation is suspended. An output signal is provided to indicate the suspend status of the programming operation.

20 A method is also described for providing the protection status of a data modification operation in a memory device. A data modification operation is issued with respect to a memory location. The protection status of the memory location is determined. An output signal is provided to indicate the protection status of the memory location.

25 Other features and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description that follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:

5 Figure 1 illustrates a prior art status register.

Figure 2 illustrates a computer system that includes one embodiment of the memory device.

Figure 3 illustrates a CPU coupled to one embodiment of the memory device.

10 Figure 4 illustrates one embodiment of the status register.

Figure 5 illustrates a flow chart for initializing one embodiment of the status register.

Figure 6 illustrates a flow chart for performing a programming or erase operation for one embodiment of the memory device.

15 Figure 7 illustrates a flow chart for performing a block lock check for one embodiment of the memory device.

Figures 8 through 12 illustrate a flow chart for a programming operation.

Figures 13 through 17 illustrate a flow chart for an erase operation.

DETAILED DESCRIPTION

One embodiment of the memory device optimizes the memory to processor interface by providing a programming suspend status signal. The programming suspend status signal is used to indicate the current execution status (i.e., whether a programming operation is suspended or is not suspended) of a programming operation. For one embodiment, the programming operation is a byte write operation. Once the processor is informed that the execution of the current programming operation is suspended, the processor may request that a different read, program or erase operation may be performed while the programming operation is suspended.

For example, once the processor is informed that the programming operation to a specific memory location is suspended, then the processor may request that a read operation be performed on another memory location. As such, the processor may not be required to wait until the entire programming operation to a first memory location is completed (which may be an unacceptable time) before reading from a second memory location. In certain situations, this feature may improve the efficiency of the computer system.

One embodiment of the memory device optimizes the memory to processor interface by providing a protection status signal. This signal is used to indicate whether the memory location accessed by a program or erase operation resides in a protected memory block or an unprotected memory block.

For one embodiment, a protected memory block is referred to as a locked memory block and an unprotected memory block is referred to as an unlocked memory block. The data stored in an unlocked memory block may be modified by a program or erase operation; however, the data stored in a locked memory block may not be modified unless the memory block is first

unlocked by an override operation. This feature of providing a protection status signal typically allows the processor to differentiate between a program or erase operation that failed due to an attempt to access a memory location in a memory block that was protected (e.g., block locked) versus a program or
5 erase operation that failed due to a power failure or a bad block. One intent is to improve the efficiency of the computer system.

The purpose of the protection status signal is to provide the user with meaningful information about an operation. If the user finds out that the operation (for example, a byte write operation) failed because of block
10 protection, the user can unlock the block and reissue the command. But if the operation failed because of a bad block, then the user will not try to write again to the same location. That is why the differentiation between the two types of failures is advantageous. An analogy would be being unable to open a car door because the door is locked versus because the door is jammed. In
15 the former case, one uses a key to open the door. In the latter case, one calls a mechanic to fix the door.

One embodiment of the memory device may be used in various types of computer systems or data processing systems. The computer system within which the memory device, such as a flash memory device, is used can be a
20 personal computer, a notebook computer, a laptop computer, a personal assistant/communicator, a minicomputer, a workstation, a mainframe, a multiprocessor computer, or any other type of computer system. In addition, the system in which the memory device is used can be a printer system, a cellular phone system, a digital answering system, a digital camera, or any
25 other system that requires data storage.

Figure 2 illustrates one embodiment of a general purpose computer system 10. The computer system 10 may include a power supply 11, a central

processing unit ("CPU") 12, a main memory 13, a flash memory 14, a mass storage device 15, a frame buffer 16, and an input device 18, all of which are coupled to a bus 19. Data may be transferred among the various components in the system 10 via the bus 19. The frame buffer 16 receives image data which are displayed on the display device 17.

For one embodiment, the mass storage device 15 is a "solid state disk drive" that includes a plurality of flash EEPROM devices for emulating the operation of a magnetic hard disk drive. For another embodiment, the mass storage device 15 is a hard disk drive.

The power supply 11 includes a VCC output that provides the VCC operating voltage to the various components in the system via the bus 19. The power supply 11 may also include a VPP output that provides the VPP programming voltage to flash memory 14 and flash memory within mass storage device 15.

Figure 3 illustrates one embodiment of a block diagram of a flash memory device 200 coupled to a CPU 201 in a computer system. The flash device 200 includes a main memory array 212, which is subdivided into multiple memory blocks (i.e., block 1 through block N). For one embodiment, the main memory 212 stores 1 megabyte of data with each byte storing 8 bits of data. The 1 megabyte of data may be arranged in sixteen 64 kilobyte memory blocks which are individually erasable, lockable, and unlockable in the computer system. The Y decoding and gating circuit 210 and the X decoding circuit 211 may be used to select the memory locations within the main memory array 212 that are accessed by the CPU 201.

For one embodiment, main memory 212 includes flash memory cells that include electrically isolated gates referred to as floating gates. The flash memory cells include a drain region and a source region in a substrate. A

polysilicon gate is generally disposed above and between these regions and insulated from these regions by an insulating layer. A second gate, referred to as the floating gate, is disposed above the floating gate and may be fabricated from a second layer of polysilicon. The gate terminals of the flash memory cells are coupled to the word-lines and the drain terminals of the flash memory cells are coupled to the bit-lines.

The flash memory device 200 includes a block lock mini-array 214 for storing bits referred to as the block lock bits. As noted above, the setting and clearing of the block lock bits is used to prevent or protect data stored in the main memory array 212 from being modified. The Y decoding and gating circuit 213 and the X decoding circuit 215 is used to select the memory locations within the block lock mini-array 214 that are accessed by the CPU 201.

For one embodiment, the protection mechanism incorporating the block lock bits uses a combination of bits, sixteen block lock bits and a master lock bit, to lock and unlock the various memory blocks. The locked block lock bits gate attempts to perform block erase or programming operations, while a locked master lock bit gates attempts to modify the block lock bits. Various lock bit configuration operations (i.e., set block lock bit, set master lock bit, and clear block lock bits commands) are used to configure the bits in the block lock mini-array. For an alternative embodiment, the mini-array 214 is used to store data other than the block lock bits.

When the CPU 201 accesses a memory location for an operation (e.g., read operation, write operation, erase operation, etc.), the address signals generated by the CPU 201 are received by the flash memory device 200 via the address bus 220. The address signals are inputted directly into the multiplexer ("mux") 217 or inputted into the address latch 216. The address latch 216 is

coupled to the mux 217 to provide address signals to the mux 217 via the internal bus 221. The command state machine ("CSM") 203 provides a control signal to the mux 217 to select between the input coupled to the address bus 220 and the input coupled to the address latch 216. The mux 217 provides the address signals generated by the CPU 201 over the internal bus 228 to the appropriate decoding circuits (i.e., Y decoding and gating circuit 213, X decoding circuit, Y decoding and gating circuit 210, and X decoding circuit 211).

The CSM 203, also referred to as the command user interface ("CUI"), serves as the interface between the CPU 201 and the internal operation of the flash memory device 200. Commands are written into the CSM 203 using standard microprocessor write timings. The CSM 203 contents serve as an input to the internal write state machine ("WSM") 205, which controls the various data modification operations of the flash memory device 200. For one embodiment, the CSM 203 controls the block erase, byte write, and lock bit configuration operations. Functions associated with altering the data in the memory arrays (e.g., block erase, byte write, lock bit configuration, and status operations) are accessed via the CSM 203 and are executed under the control of the WSM 205. Data stored in the memory arrays 212 and 214 or data stored in the status register 206 may be accessed by inputting the appropriate commands into the CSM 203. The CSM 203 and the WSM 205 are referred to as the control logic.

Once a valid command or command sequence has been generated by the CPU 201 and written into the CSM 203, the flash memory device 200 automatically executes the command or commands. In other words, the control logic automatically executes the algorithms and timings necessary for the various data operations.

The CPU 201 programs (i.e., writes) data into the flash memory device 200 via the data bus 223. Data bus 223 is coupled to the data input/output pins (e.g., DQ₀-DQ₇). The data to be written into the main memory array 212 or the block lock mini-array 214 is inputted into the data latch 204 via the data bus 223 when the appropriate control signals (e.g., \overline{WE}) are received from the CPU 201, and subsequently inputted into the write state machine 205 via the internal bus 220. When the CSM 203 provides the control signals to the WSM 205 via the line 270, the WSM 205 provides the appropriate program control signals over line 290 to the voltage control circuit 209. In response to the program control signals from the WSM 205, the voltage control circuit 209 provides the appropriate voltage signals to the flash memory cells selected (i.e., addressed) for programming. For one embodiment, flash memory cells may be programmed by applying 12 volts to the gate terminal of the flash memory cell via the selected word-lines, 6 volts to 7 volts to the drain terminal of the flash memory cell via the selected bit-lines, and by applying ground to the source terminal of the flash memory cell.

For one embodiment, the data operations of writing or programming data into the memory arrays are performed in byte increments and thus are referred to as byte write operations. For one embodiment, a byte write operation takes approximately 6 μ s when V_{cc} is at 5 volts and V_{pp} is at 12.0 volts. One embodiment of the flash memory device 200 may also operate in the byte write suspend mode. The byte write suspend mode enables the system to read data or execute code from any other memory location within the flash memory array while the byte write operation is suspended.

Data stored in the memory arrays (e.g., main memory array 212, block lock mini-array 214) may be erased by applying the appropriate voltage signals to the selected memory cells. During an erase operation, the CSM 203

receives an erase command via the data bus 223 and the CE# and WE# control signals from the CPU 201. Once the CSM 203 provides erase control signals to the WSM 205, the WSM 205 may enable the voltage control circuit 209 to provide the appropriate voltage signals to the selected memory cells.

- 5 For one embodiment, a block of memory cells may be erased by applying -11 volts to gate terminal of the flash memory cells, 6 volts to the source terminal of the flash memory cells, and by floating the drain terminal. For one embodiment, an entire block may be erased within 1 second.

The CPU 201 reads data stored in the memory arrays (e.g., main
10 memory array 212, block lock mini-array 214) via the data bus 223. The main memory array 212 is coupled to the sense circuit 207 via the bus 230, and the block lock mini-array is coupled to the sense circuit 208 via the bus 229. The sense circuit 207 is used to sense the bit-line voltages of the selected and non-selected memory cells in the main memory array 212. Similarly, the sense
15 circuit 208 is used to sense the bit-line voltages of the selected and non-selected memory cells in the block lock mini-array 214. The sense circuit 207 provides data signals over the bus 227 to the output multiplexer ("mux") 202 and the sense circuit 208 provides data signals over bus 225 to the output mux 202. These data signals represent the data read from the selected memory
20 locations. For one embodiment, each memory location accessed for a read operation includes eight bits. When the output mux receives the appropriate read control signals via line 254 from the CSM 203 and receives an asserted output enable ("OE") signal from the CPU via line 264, the output mux 202 outputs the data signals onto the data bus 223. The CPU 201 then accesses the
25 data from the data bus 223.

The flash memory device 200 also includes a status register 206. The status register 206 includes any type of storage device that is capable of storing

the status information. For one embodiment, the status register 206 includes multiple flip-flop circuits. Although Figure 3 shows the status register 206 residing outside of CSM 203, for an alternative embodiment, status register 206 resides within the CSM 203 or the control logic.

5 Status register 206 indicates when the WSM 205 has completed a block erase, byte write, or block lock bit configuration operation. Furthermore, the status register 206 indicates whether these operations have been completed successfully or unsuccessfully. Status register 206 also provides other status signals, such as a byte write suspend status signal that indicates whether a byte
10 write operation has been suspended or a protection status signal to indicate whether a byte write operation, a block erase operation, or a block lock bit configuration operation has failed due to attempts to modify a "locked" memory location.

 The CPU 201 accesses the data stored in the status register 206 by
15 providing a read status register command over the data bus 223. In response to a read status register command, the CSM 203 provides a read status register control signal over line 253 to the status register 206. The requested status data from the status register 206 is outputted onto the internal bus 226. When the control signals generated by the CSM 203 and received by the output mux
20 202 over line 254 enables the output mux 202 to select the data from the internal bus 226, the requested status data is then outputted from the flash memory device 200 via the data bus 223.

 The status register 206 stores multiple memory bits, and one or more of the memory bits is used to provide a specific status signal. The status signal is
25 outputted from the flash memory 200 via an output pin designated to provide a certain status signal or via the data input/output pins (e.g., DQ₀-DQ₇). For one embodiment, the flash memory device 200 includes a

READY/BUSY# (RY/BY#) pin to indicate whether the flash memory device is ready to receive a new command or is busy performing the previous command. The processor polls the RY/BY# pin to determine the status of the RY/BY# pin. For an alternative embodiment, the status of a specific status signal is read via the data input/output pins (e.g., DQ₀-DQ₇) of the flash memory device 200 after inputting a read status register command via the data input/output pins.

Figure 4 illustrates one embodiment of the status register 206. The status register 400 includes eight memory locations 401 through 408. Each of the memory locations stores at least one memory bit and provides at least one status signal. Similar to the prior art status register 100, the status register 400 stores the Vpp status ("VPPS") information, the byte write and set lock bit status ("BWSLBS") information, the erase and clear lock bits status ("ECLBS") information, the erase suspend status ("ESS") information, and the write state machine status ("WSMS") information. More specifically, memory location 404 stores the VPPS information. Memory location 405 stores the BWSLBS information. Memory location 406 stores the ECLBS information. Memory location 407 stores the ESS information. Memory location 408 stores the WSMS information.

In addition to storing the status information for the VPP, BWSLBS, ECLB, ES, and WSM, the status register 400 includes additional memory locations for storing the status information related to the suspension of a programming operation and/or the protection of a memory location (or locations) addressed for a data operation. For one embodiment, the status register stores write byte suspend status ("WBSS") information and/or the data protection status ("DPS") information. The number of total memory locations may vary for alternative embodiments. Furthermore, the status

register 400 may include one or more additional memory locations, such as the memory location 401, which is designated as a reserved memory location. A reserved memory location is a memory location that is not currently being used to store status information but may be reserved to store status
5 information in the future.

One embodiment of the flash memory device 200 allows the system software to suspend a programming operation in order to read data from another flash memory array location. A programming operation is suspended by entering a programming suspend command. For one
10 embodiment, a programming operation is referred to as a byte write operation. The programming operation is suspended by entering a byte write suspend command. Once the programming process starts, a programming suspend command causes the control logic to suspend the byte write sequence at one of the predetermined points in the algorithm. The BWSS information
15 indicates whether the programming operation is suspended or not suspended in response to the programming suspend command.

One embodiment of the flash memory device 200 stores DPS information. When a data modification operation (i.e., a program or erase operation) is requested, a protect status signal is outputted from the flash
20 memory device 200 to inform the CPU (or other devices) that the attempted data modification operation addressed a protected memory location (e.g., a locked memory location) or an unprotected memory location (e.g., an unlocked memory location). For one embodiment, when the requested data modification operation fails, the user is able to distinguish between an
25 operation failure due to locked memory block versus an operation failure due to other failures, such as power failure or a bad block. This allows the user to

be better informed as to the causes of the failure so the user can better react to the failure.

For example, if the requested data modification operation failed due to an attempt to modify data in a locked memory block, the user may decide to modify data in another memory block that is unlocked or the user may decide to unlock the memory block in order to modify the data. On the other hand, if the requested data modification operation failed due to a bad block, the bad block may be replaced with a redundant block or the flash memory device 200 may be designated as a failed device.

The following figures illustrate the steps involved in providing the various status signals. For one embodiment, the status register 400 is initialized according to the steps shown in Figure 5. The flash memory device 200 is powered-up by applying the appropriate power supply signals as shown in step 501. For one embodiment, the flash memory device 200 operates with a 3.3 volt or a 5.0 volt VCC power supply. For an alternative embodiment, the flash memory device operates with a 1.8 volt VCC power supply.

Once the flash memory device 200 is powered-up, the RESET/DEEP POWER-DOWN (RP#) input pin is checked, as shown in step 502. For one embodiment, the RP# pin is used for placing the flash memory device 200 in the deep power-down mode and for resetting the internal automation of the flash memory device 200. A logic high voltage level on RP# enables the normal operation of the flash memory device 200 and a logic low voltage level on RP# inhibits any operations in order to provide data protection during power transitions and to save power. If RP# is at a logical high level, then the memory locations 402 through 408 are initialized as shown in step 503. For one embodiment, the memory locations 402 through 407 are

initialized by being set to "0" and the memory location 408 is initialized by being set to "1."

When the status register 400 is initialized, the memory location 402 indicates an unlocked protection status. Memory location 403 indicates a byte
5 write operation is in progress or completed. Memory location 404 indicates that the Vpp voltage is at an appropriate voltage level. Memory location 405 indicates a successful byte write operation or set master/block lock bit operation. Memory location 406 indicates a successful block erase operation or clear lock bits operation. Memory location 407 indicates a block erase
10 operation is in progress or is completed. Memory location 408 indicates that the control logic is ready to receive a new command or command sequence.

Figure 6 illustrates a flow chart for performing a programming or erase operation for one embodiment of the flash memory device 200. According to step 601, a programming command or an erase command is received by the
15 flash memory device 200. The programming command or the erase command may include a sequence of commands. Typically, these commands are generated by the CPU 201.

If a programming command (or sequence of commands) is received, the address of the memory location to be written to and the data to be written
20 is received by the flash memory device 200, as shown in step 602. If an erase command is received, the address of the memory location (i.e., memory block) to be erased is received by the flash memory device 200, as shown in step 602. After steps 601 and 602 are completed, the control logic controls the programming and programming verify algorithms internally (not shown).
25 Similarly, the control logic controls the erase and erase verify algorithms internally (not shown).

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The flash memory device 200 then performs a block lock check in step 603. The block lock check includes a sequence of steps that update the status register (e.g., the memory location 402, which stores the protection status information). The block lock check is described in more detail in connection with Figure 7.

Next, the control logic determines whether the block lock bit, corresponding to the memory location to be accessed, is set. If the block lock bit is not set, then the programming or erase operation is performed in step 605 and the programming or erase operation is verified in step 607. On the other hand, if the block lock bit is set, then the flash memory device 200 determines whether or not to override the setting of the block lock bit corresponding to the memory location addressed for a write or erase operation, as shown in step 606. For one embodiment, the override command may be enabled by RP# being at 12 volts. If the override is not enabled and the block lock bit is set, then the programming or erase operation fails due to a locked memory block.

On the other hand, if the override is enabled and the set block lock bit is cleared, then the programming or erase operation is performed at step 605 and then verified as having been successfully performed in step 607. If it is determined in step 607 that the programming or erase operation was not successful, then the flash memory device 200 indicates that the programming or erase operation failed for reasons other than an attempt to access a memory location residing within a locked memory block, as shown in step 609. For example, the failure may have been caused by a performing an erase or programming operation on a bad or defective memory block or a power failure. Otherwise, the flash memory device 200 indicates that the programming or erase operation was successfully completed.

The block lock check step 603 is described in more detail in Figure 7. For one embodiment, each lock bit corresponds to a block of memory in the main array, and therefore, the lock check may be referred to as a block lock check. As previously mentioned, the flash memory device 200 includes a
5 block lock mini-array 214 for storing bits referred to as the block lock bits. The setting and the clearing of the block lock bits is used to prevent or protect data stored in the main memory array 212 from being modified. For one
embodiment, each block lock bit in the mini-array 214 corresponds to a respective block of memory cells in the main memory array 212. The
10 programming (i.e., the setting or clearing) of the bits in the block lock mini-array 214 is described below in conjunction with Figure 8.

According to step 701, the flash memory device 200 reads the block lock bit in the mini-array 214 that corresponds to the memory block in the main array 214 that includes the memory location selected (i.e., addressed) for a
15 programming or erase operation. For one embodiment, the memory location addressed for a programming operation is a byte of data and the memory location addressed for an erase operation is a block of data. Step 701 typically occurs while the control logic is executing the command sequence for the programming operation or the erase operation.

20 While performing the block lock check, the control logic within the flash memory device 200 determines at step 702 whether the block lock bit is set. For one embodiment, a cleared lock bit is at a logic "0." A set lock bit is at a logic "1." If the corresponding block lock bit is set, then the control logic updates the status register 206 to indicate that the corresponding block lock bit
25 is protected or locked. For one embodiment, memory location 402 is updated to indicate that the memory block selected for a data modification operation is locked.

On the other hand, if the corresponding block lock bit is not set, then the control logic updates the status register 206 to indicate that the corresponding block lock bit is not locked. For one embodiment, the memory location 402 is updated to indicate that the memory block selected for a data modification operation is unlocked.

Figure 7 illustrates in step 702 that if the corresponding block lock bit is not set, then the block lock check is completed. For one embodiment, the DPS information in the status register 206 has already been initialized to indicate that the block lock bits are not set. Thus, when it is determined that the lock bit corresponding to the addressed memory location is not set, the DPS information does not need to be modified.

Figures 8 through 12 provide a detailed description of the programming operation for one embodiment of the flash memory device 200. Unlike the prior art flash memory devices, one embodiment may distinguish between a programming or write operation failure due to a device protect error and a program operation failure (such as a power failure or a bad block). Furthermore, unlike the prior art flash memory devices, one embodiment, allows the flash memory device 200 to suspend a programming operation.

For one embodiment, the main memory array 212 is programmed by performing a programming operation such as a byte write operation. In step 901, the control logic receives a programming command, such as a byte write command, to initiate the programming operation. Once the data to be written and the address to be written into the flash memory device 200 is received by the control logic in step 902, the status register 206 is updated to indicate that the control logic is busy performing a data modification operation in step 903. For one embodiment, the memory location 408 in the status register 400 is updated to store a logic "0."

Once the status register 206 has been updated at step 903, the control logic performs a block lock check at step 904. The block lock check in step 904 is performed in accordance with the steps described in Figure 7. The block lock check ensures that the status register 206 includes the updated protection status information corresponding to the memory location selected for the programming operation. Next, in step 905, the control logic starts performing the programming operation specified by the programming command.

The control logic then determines if the programming operation is completed in step 1001. If the programming operation is completed, then the status register 206 is updated to indicate that the control logic has completed its previous data modification operation and is ready to receive a new data modification operation in step 1002. After updating the status register 206, a determination is made in step 1003 whether to perform a full status check. The full status check checks the various status signals to determine whether a specified failure has occurred. Figure 12 describes the status check in more detail. If a full status check is desired, then the control logic proceeds to step 1301. Otherwise, the programming operation is completed.

On the other hand, if the programming operation is not completed in step 1001, then the control logic determines whether a programming suspend command has been entered in step 1004. If a programming suspend command has been entered, then the control logic proceeds to step 1101 in Figure 10.

Once a programming suspend command has been entered, the control logic may or may not proceed to suspend the programming operation. The programming suspend command requests that the control logic suspend the programming operation sequence at one of the predetermined points in the algorithm. Although a programming suspend command has been received

by the control logic, if the program operation has already or is currently executing those commands, the programming operation may not be suspended.

If the programming operation is not suspended, the control logic returns to step 1001 to determine if the programming operation is completed. On the other hand, if the programming operation is suspended, the control logic proceeds to step 1002 to update the status register 206 to indicate that the programming operation is suspended. For one embodiment, the memory location 403 is updated to store a logic "1" to indicate the programming operation (e.g., byte-write operation) is suspended. Once the status register 206 is updated to indicate that the programming operation is suspended, the status register 206 is updated to indicate that the control logic is ready to perform a new data modification operation, as shown in step 1103. For one embodiment, the memory location 408 in the status register 206 stores the WSMS information.

Once the status register 206 is updated, the control logic receives a read status register command as shown in step 1104. In response to the read status register command, the flash memory device 200 automatically outputs the WSMS signal and the BWSS signal. After the WSMS signal is outputted from the flash memory array 200, the flash memory array 200 receives a read command for a memory location other than that specified by the write operation that was suspended. In other words, a read operation may not be performed on the same memory location that was specified in the programming operation that is currently being suspended.

Next, a read operation is performed on the selected memory location in the main memory as shown in step 1106. The control logic determines when the read operation is completed in step 1106. Once the control logic has

completed the read operation, the control logic proceeds to perform step 1201 as shown in Figure 11.

Once the read operation is completed, the flash memory device 200 receives a programming resume command at step 1201. The control logic
5 then updates the status register 206 to indicate that the control logic is busy completing the programming or write operation. Additionally, the status register 206 is updated at step 1203 to indicate that the programming operation is no longer suspended. For one embodiment, the memory location 408 and the memory location 403 in the status register 400 are each updated to store a
10 logic "0." After steps 1202 and 1203 are completed, step 1001 is repeated.

Referring back to step 1003 in Figure 9, if the flash memory device 200 determines that a full status check is to be performed, the flash memory device 200 proceeds to step 1301 in Figure 12. At step 1301, the control logic receives a read status register command. For one embodiment, the memory
15 location 404 (which stores the VPPS information), the memory location 402 (which stores the DPS information), and the memory location 405 (which stores the BWSLBS information) may be read from the status register 206.

These memory locations within the status register 206 are read to determine the various failures modes. At step 1302, the flash memory device
20 200 checks whether the programming voltage V_{pp} applied to the flash memory device 200 is within the appropriate voltage level range. If V_{pp} is not within an appropriate voltage level (e.g., if V_{pp} is not greater or equal to 3 volts), then the VPPS signal indicates a V_{pp} range error in step 1305. On the other hand, if V_{pp} is within the appropriate range, then another status check
25 is made.

The flash memory device 200 also checks whether the programming operation is requested to be performed on a memory location within a locked

memory block in step 1303. If the selected memory location resides within a memory block that is device protected or locked, then a device protect error results, as shown in step 1306. On the other hand, if the selected memory location resides within an unprotected or unlocked memory block, then
5 another status check is made.

At step 1304, the flash memory device 200 checks whether the programming operation was performed successfully. If the programming operation was not successfully completed, then the flash memory device 200 at step 1307 detects a program operation error in step 1307 and the code
10 terminates. On the other hand, if the programming operation was successfully completed, then the full status check is completed. For an alternative embodiment, another status check may be made, however.

Figures 13 through 17 describe an erase operation for one embodiment. Unlike the prior art flash memory devices, one embodiment distinguishes
15 between an erase operation failure due to a device protect error and a failure due to an erase operation failure (e.g., a bad memory location).

Once the flash memory device 200 receives an erase command (or command sequence) in step 1401 and the address of the memory location to be erased in step 1402, the status register 206 is updated at step 1403 to indicate
20 that the control logic is busy performing an erase operation. For one embodiment, the memory location 408 in the status register 206 is updated to store a logic "0."

Next, the control logic performs a block lock check as shown in step 1404. For one embodiment, the block lock check is performed in accordance
25 with the steps provided in Figure 7. After the block lock check is completed, the control logic proceeds to start the erase operation.

Next, step 1501 in Figure 14 determines whether the erase operation is completed. If the erase operation is completed, then at step 1502 the status register 206 is updated to indicate that the control logic is ready to perform a new data modification operation. For one embodiment, memory location 408 is updated to store a logic "1." The flash memory device 200 then determines at step 1503 whether to perform a full status check. If a full status check is not performed, the erase operation is completed. Otherwise, the control logic proceeds to perform the full status check. For one embodiment, the full status check is performed according to the steps described in Figure 17.

On the other hand, if it is determined at step 1501 that the erase operation is not completed, then the control logic determines whether the control logic has received an erase suspend command. If an erase suspend command has not been entered, then step 1501 is repeated. Otherwise, the control logic proceeds to step 1601 in Figure 15.

An erase operation is suspended at designated points in the erase operation algorithm. Once an erase suspend command has been received by the flash memory device 200, the control logic may or may not suspend the erase operation, depending on what stage the control logic is at in performing the erase operation. If the erase operation is not suspended, then step 1501 is repeated. Otherwise, the control logic updates the status register 206 to indicate that the erase operation is suspended, as shown in step 1602, and the control logic is ready to perform a new data modification operation, as shown in step 1603. For one embodiment, the memory location 407 in the status register 400 is updated to store a logic "1" and the memory location 408 in the status register is updated to store a logic "1."

At step 1604, the control logic receives a read status register command. Once the status register 206 indicates that the control logic is ready to perform

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a new data modification operation, the control logic receives a read or programming command, as shown in step 1603. Subsequently, the read operation or programming operation is performed in step 1606.

After the read or program operation is completed in step 1606, step 1701 is performed as, shown in Figure 16. At step 1701, the control logic receives an erase resume command. Next, the status register 206 is updated to indicate that the control logic is busy performing the erase operation because the erase operation is no longer suspended. For one embodiment, the memory location 408 is updated to store a logic "0" and the memory location 407 is updated to store a logic "0." Step 1501 is then repeated.

The steps in Figure 17 are performed if it is determined in step 1503 that the a full status check is to be performed. The full status check in step 1503 is used to determine the various failure modes. The control logic receives the read status register command in step 1801. For one embodiment, memory location 404 (which stores the VPPS information), memory location 402 (which stores the DPS information), memory location 406 (which stores the ECLBS information), and memory location 405 (which stores the BWSLBS information), are read during the full status check.

A programming voltage V_{pp} range error is detected in step 1806 when the status register 206 indicates that the V_{pp} level is not in the appropriate range in step 1802. A device protect error 1807 is detected in step 1807 when the status register indicates that the attempted erase operation requested a protected or locked memory block to be modified, as shown in step 1803. A command sequence error is detected in step 1808 if at step 1804 both the memory locations 405 and 406 are found to be set to a logic "1." An erase operation error is detected in step 1809 when the status register indicates that the erase operation was not successfully completed. For one embodiment, the

full status check is completed after performing the four status checks described above.

In the foregoing specification, the invention has been described with references to specific embodiments thereof. It will, however, be evident that
5 various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense.

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CLAIMS

What is claimed is:

1 1. A memory device, comprising:
2 a memory array;
3 a register configured to store at least one bit indicating a suspend status
4 of a write operation; and
5 a control circuit coupled to said memory array and said register, said
6 control circuit configured to update said register and to control the output of a
7 status signal representing said suspend status of said write operation.

1 2. The memory device of claim 1, wherein said register resides
2 within said control circuit.

1 3. The memory device of claim 1, wherein said control circuit is
2 configured to receive a status request signal and said register is configured to
3 output said status signal in response to said status request signal, said status
4 signal having a first state to indicate said write operation is suspended and a
5 second state to indicate said write operation is not suspended.

1 4. The memory device of claim 3, further comprising at least one
2 data input/output coupled to said control circuit, wherein at least one data
3 inputs/output is configured to receive said status request signal from a
4 processor and to provide said status signal to said processor.

1 5. The memory device of claim 1, further comprising a status
2 output coupled to said register, wherein said status output is configured to

3 provide a second status signal when said status output is polled, said second
4 status signal having a first state to indicate said write operation is suspended
5 and a second state to indicate said write operation is not suspended.

1 6. The memory device of claim 5, wherein said status output
2 represents an output pin.

1 7. The memory device of claim 1, wherein said write operation
2 represents a byte write operation.

1 8. The memory device of claim 1, wherein said control circuit
2 includes a first state machine configured to update at least one of said bits
3 indicating said suspend status of said write operation in response to a suspend
4 signal.

1 9. The memory device of claim 8, wherein said suspend signal
2 represents a byte write suspend command.

1 10. The memory device of claim 8, wherein said control circuit
2 further includes a second state machine coupled to said first state machine
3 and configured to control the output said status signal in response to a status
4 request signal.

1 11. The memory device of claim 10, wherein said status request
2 signal is a read status register command.

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1 12. A memory device, comprising:
2 a memory array;
3 a register is configured to store at least one bit indicating a protection
4 status of a data modification operation; and
5 a control circuit coupled to said memory array and said register, said
6 control circuit is configured to update said register and to control the output
7 of a status signal representing said protection status of said data modification
8 operation.

1 13. The memory device of claim 12, wherein said register resides
2 within said control circuit.

1 14. The memory device of claim 12, wherein said control circuit is
2 configured to receive a status request signal and said register is configured to
3 output said status signal in response to said status request signal, said status
4 signal having a first state to indicate said data modification operation
5 attempted to access at least one memory location within a protected memory
6 block and a second state to indicate said data modification operation accessed
7 at least one of said memory locations within an unprotected memory block.

1 15. The memory device of claim 14, further comprising at least one
2 data input/output coupled to said control circuit, wherein at least one data
3 inputs/output is configured to receive said status request signal from a
4 processor and to provide said status signal to said processor.

1 16. The memory device of claim 12, wherein said data modification
2 operation is a programming operation or an erase operation.

1 17. The memory device of claim 12, wherein said control circuit
2 includes a first state machine configured to update at least one of said bits
3 indicating said protection status of said data modification operation in
4 response to a block lock configuration signal.

1 18. The memory device of claim 17, wherein said block lock
2 configuration signal includes a set block lock bit command.

1 19. The memory device of claim 18, wherein said control circuit
2 further includes a second state machine coupled to said first state machine
3 and configured to control the output said status signal in response to a status
4 request signal.

1 20. A method of providing the suspend status of a programming
2 operation in a memory device, comprising the steps of:

3 (a) performing a programming operation to a first memory
4 location;

5 (b) prior to the completion of said programming operation,
6 receiving a suspend signal;

7 (c) determining whether or not to suspend said programming
8 operation;

9 (d) if said programming operation is suspended, updating, if
10 necessary, a status register to indicate said programming operation is
11 suspended; and

12 (e) providing an output signal to indicate said suspend status of
13 programming operation.

1 21. The method of claim 20, wherein step (e) comprises the steps of:
2 (1) receiving a read status register signal; and
3 (2) providing said output signal in response to said read status
4 register signal.

1 22. The method of claim 20, wherein step (e) comprises the step of
2 providing said output signal at a dedicated status output.

1 23. The method of claim 20, further comprising the steps of:
2 (f) performing a second data modification operation to a second
3 memory location;
4 (g) after the completion of said second data modification operation,
5 updating, if necessary, said status register to indicate said write operation is
6 not suspended; and
7 (h) resuming said first data modification operation.

1 24. The method of claim 23, wherein said second data modification
2 operation is a read operation.

1 25. The method of claim 20, further comprising, prior to step (a), the
2 step of:
3 (f) initializing said status register to indicate said write operation is
4 not suspended.

1 26. A method of providing the protection status of a data
2 modification operation in a memory device, comprising the steps of:

- 3 (a) performing a data modification operation to a memory location;
- 4 (b) determining said protection status of said memory location;
- 5 (c) providing an output signal to indicate said protection status of
- 6 said memory location.

1 27. The method of claim 26, wherein step (c) comprises the steps of:

- 2 (1) receiving a read status signal; and
- 3 (2) providing said output signal in response to said read status
- 4 signal.

1 28. The method of claim 26, further comprising, prior to step (a), the

2 step of:

- 3 (d) initializing a status register to indicate said memory location is
- 4 protected from data modifications.

1 29. The method of claim 26, wherein step (b) comprises the steps of:

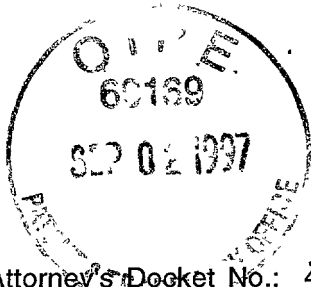
- 2 (1) performing a read operation to a location within a block lock
- 3 memory array that corresponds to said memory location; and
- 4 (2) updating a status register.

ABSTRACT OF THE DISCLOSURE

A status register for a memory device. The status register provides a programming suspend status signal and a protection status signal. The programming suspend status signal indicates whether a programming

- 5 operation is suspended. If the processor knows that a programming operation to a specific memory location is suspended, then the processor may request that a data modification operation to another memory location be performed while the programming operation is suspended. The protection status signal indicates whether an attempted data modification operation
- 10 failed due to a protected memory block versus another type of device failure. Protecting or locking a memory block prevents the modification of data stored in a particular memory block.

42390.P4024



Attorney's Docket No.: 42390.P4024

PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
STATUS INDICATORS FOR FLASH MEMORY

the specification of which

XX is attached hereto.
was filed on February 27, 1997 as
United States Application Number 08/814,928
or PCT International Application Number _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

INTEL CORPORATION
Rev. 12/11/96 (D3 INTEL) cak

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

on August 27, 1997
Date of Deposit
LESTER J. VINCENT REG # 31460
Name of Person Mailing Correspondence
Lester Vincent
Signature Date August 27, 1997

<u>Prior Foreign Application(s)</u>			<u>Priority Claimed</u>	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
_____	_____	_____	_____	_____
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
_____	_____	_____	_____	_____
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
_____	_____	_____	_____	_____

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

_____	_____
(Application Number)	Filing Date
_____	_____
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

_____	_____	_____
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
_____	_____	_____
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

45449-034T880

I hereby appoint Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; William Donald Davis, Reg. No. 38,428; Daniel M. De Vos, Reg. No. 37,813; Karen L. Feisthamel, Reg. No. 40,264; David R. Halvorson, Reg. No. 33,395; Eric Ho, Reg. No. 39,711; George W. Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; Stephen L. King, Reg. No. 19,180; Dolly M. Lee, Reg. No. 39,742; Michael J. Mallie, Reg. No. 36,591; Kimberley G. Nobles, Reg. No. 38,255; Ronald W. Reagin, Reg. No. 20,340; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Steven R. Sponseller, Reg. No. 39,384; David R. Stevens, Reg. No. 38,626; Edwin H. Taylor, Reg. No. 25,129; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Gary B. Goates, Reg. No. 35,159; Michael Anthony DeSanctis, Reg. No. 39,957; Charles E. Shemwell, Reg. No. 40,171; Edwin A. Sloane, Reg. No. 34,728; and Judith A. Szepesi, Reg. No. 39,393; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Sean Fitzgerald, Reg. No. 32,027; James E. Jacobson, Jr., Reg. No. 31,626; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Howard A. Skaist, Reg. No. 36,008; and Raymond J. Werner, Reg. No. 34,752; my patent attorneys, of INTEL CORPORATION with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Lester J. Vincent, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and
direct telephone calls to Lester J. Vincent, (408) 720-8598.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Fifth/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____

Full Name of Sixth/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____

Full Name of Seventh/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

- (1) Prior art cited in search reports of a foreign patent office in a counterpart application, and
- (2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

FIG. 1
(PRIOR ART)

100

105 WSMS	104 ESS	103 ECLBS	102 BWSLBS	101 VPPS
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FIG. 2

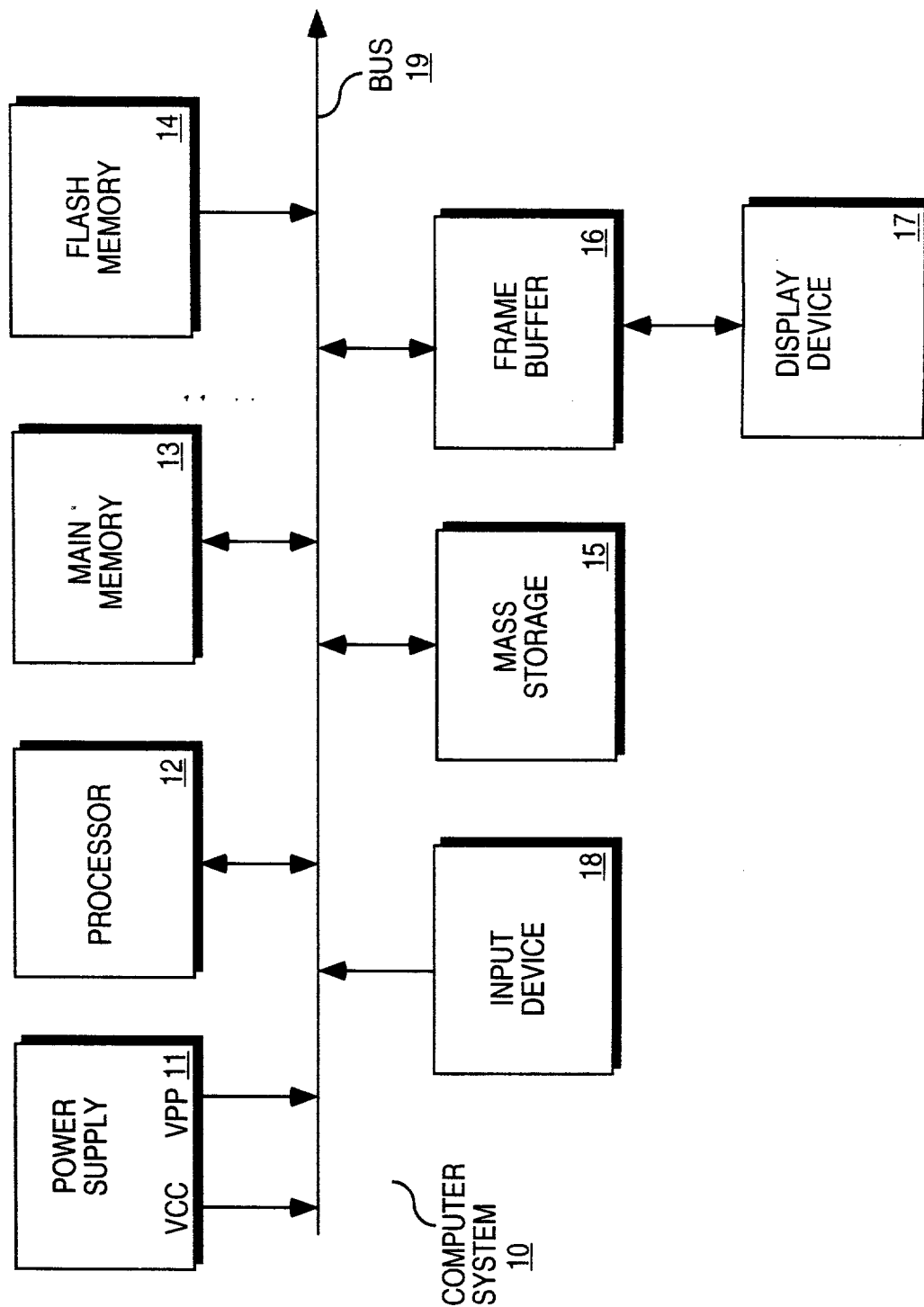


FIG. 3

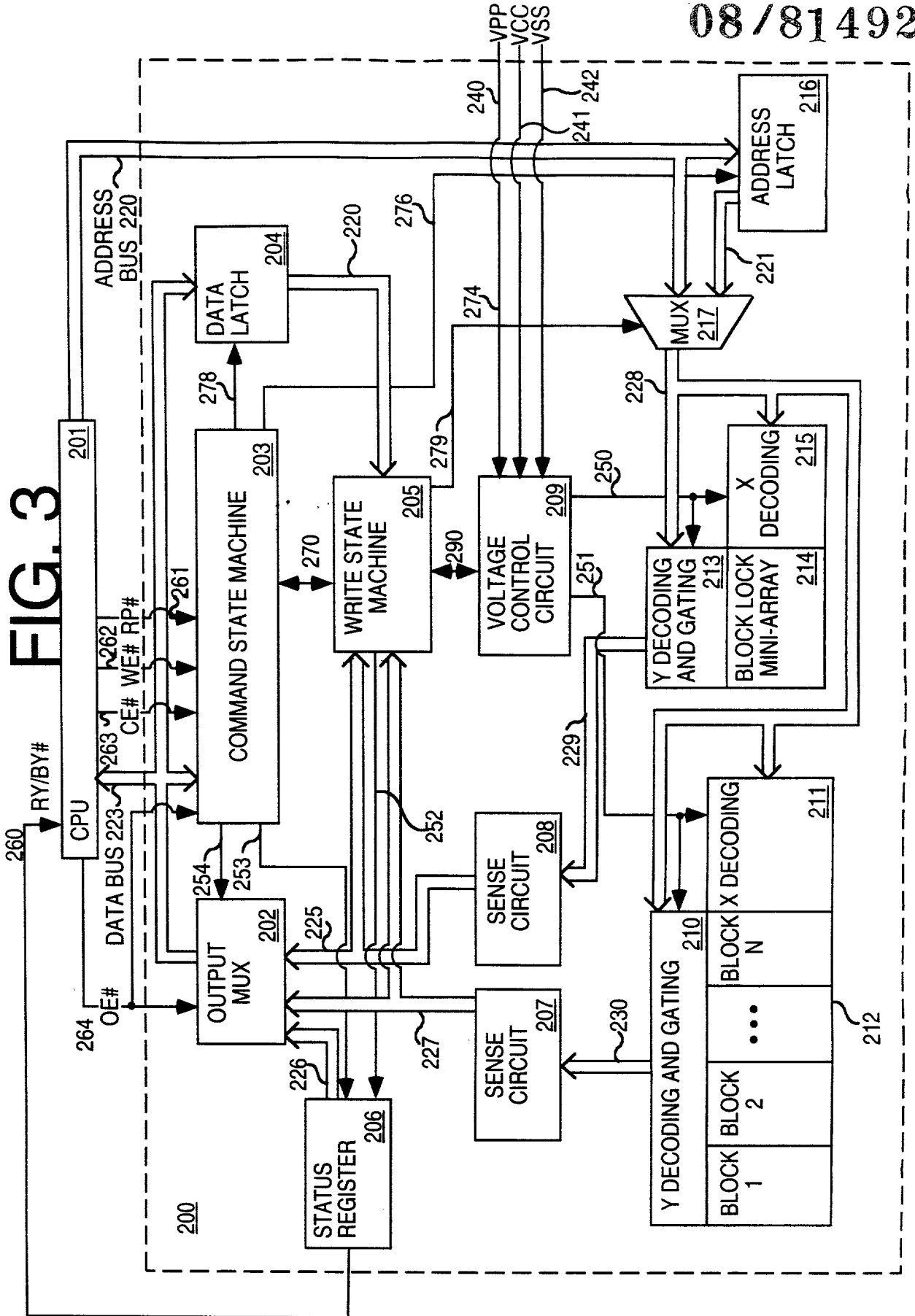


FIG. 4

400

408 WSMS	407 ESS	406 ECLBS	405 BWSLBS	404 VPPS	403 BWSS	402 DPS	401 R
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FIG. 5

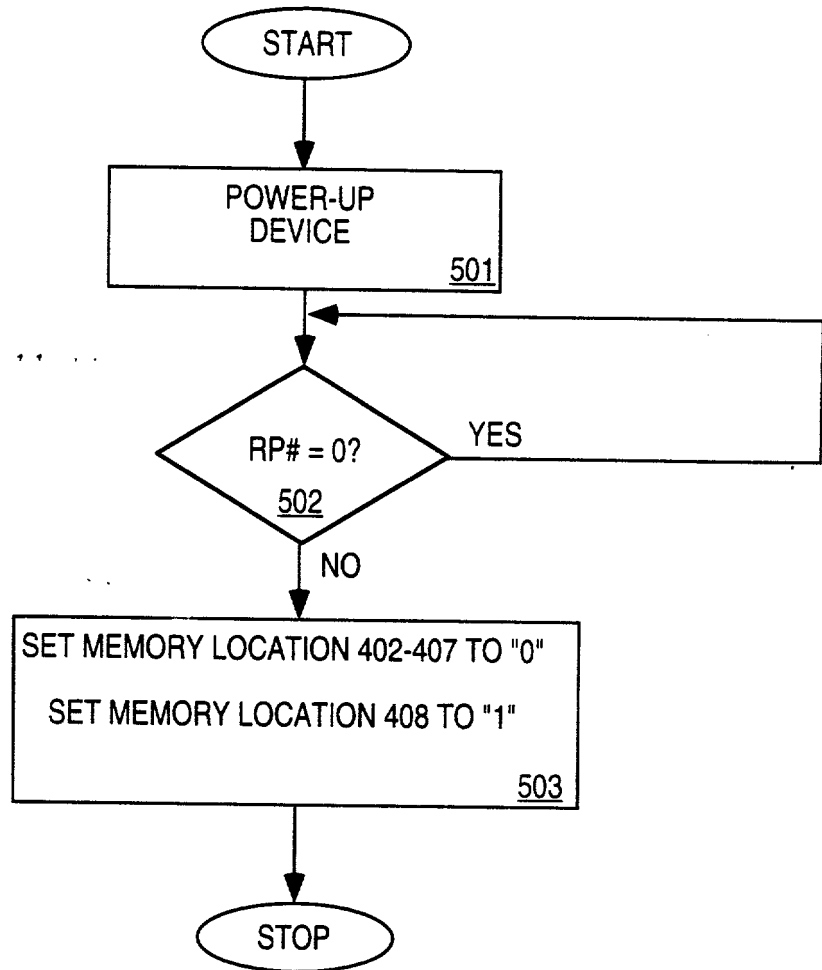


FIG. 6

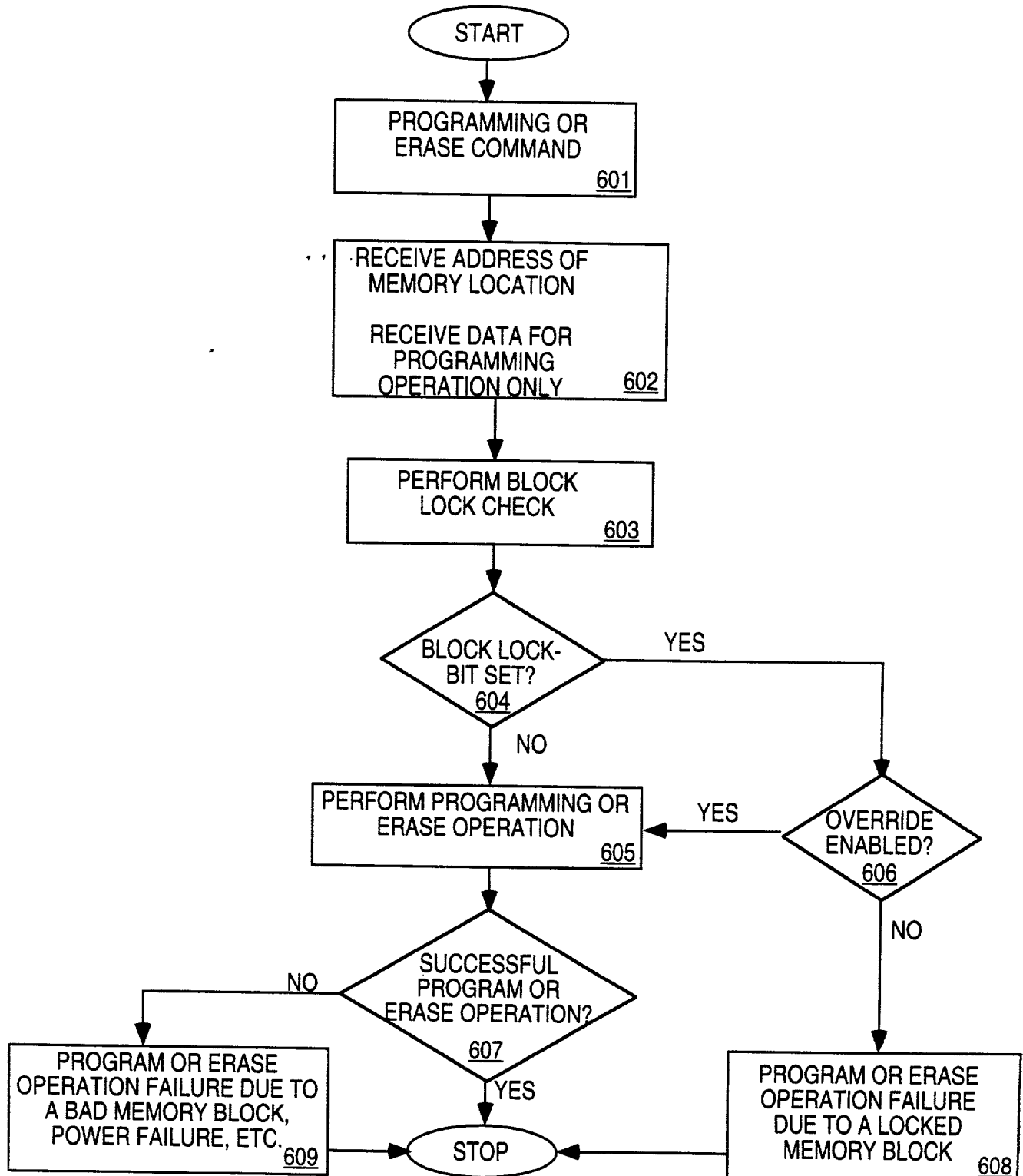


FIG. 7

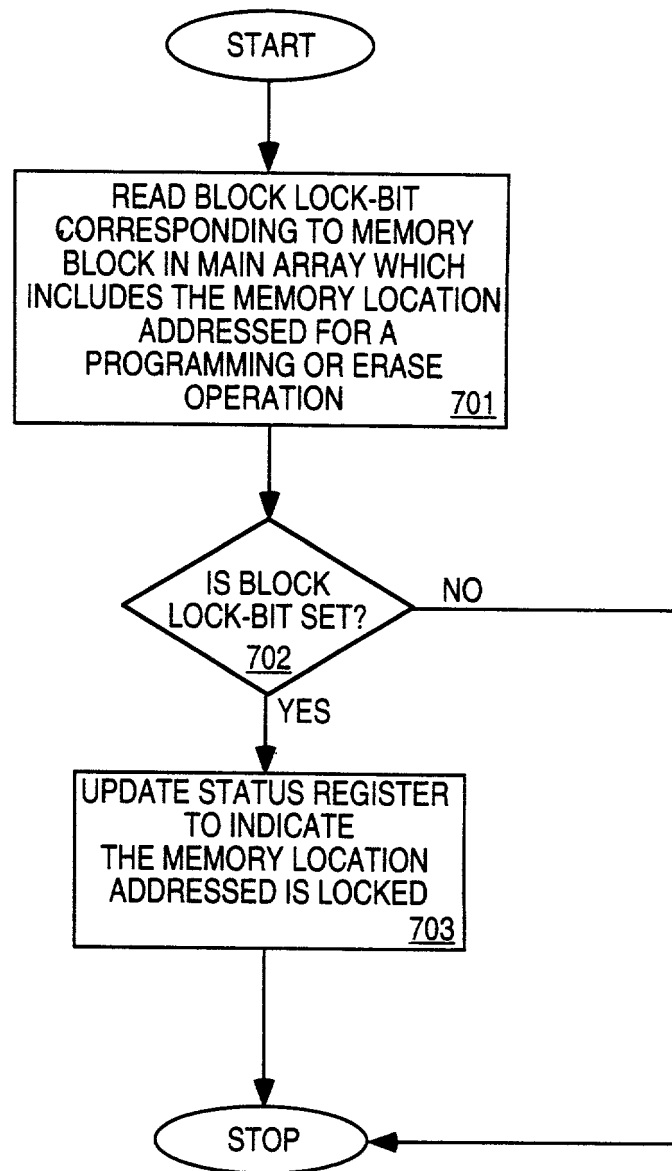


FIG. 8

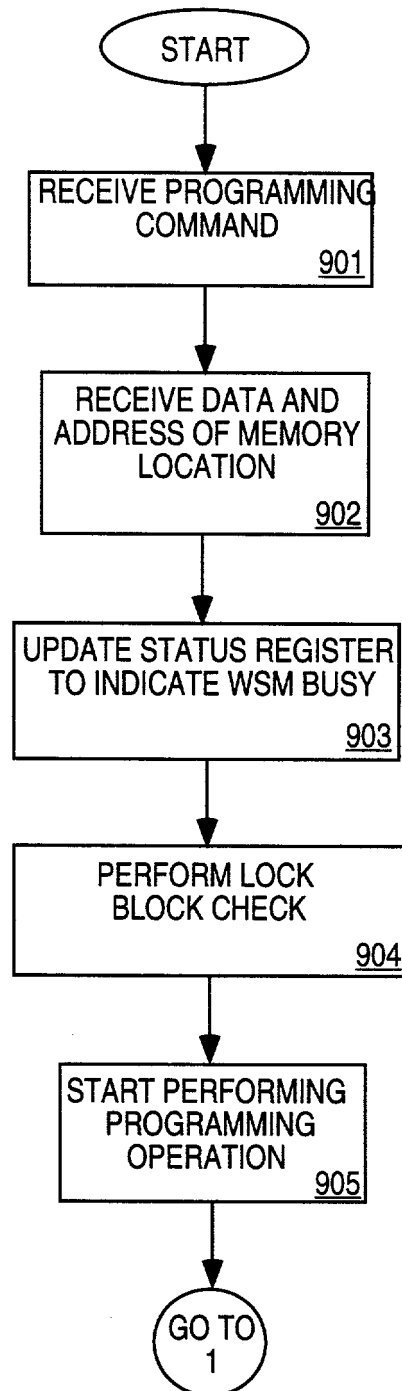


FIG. 9

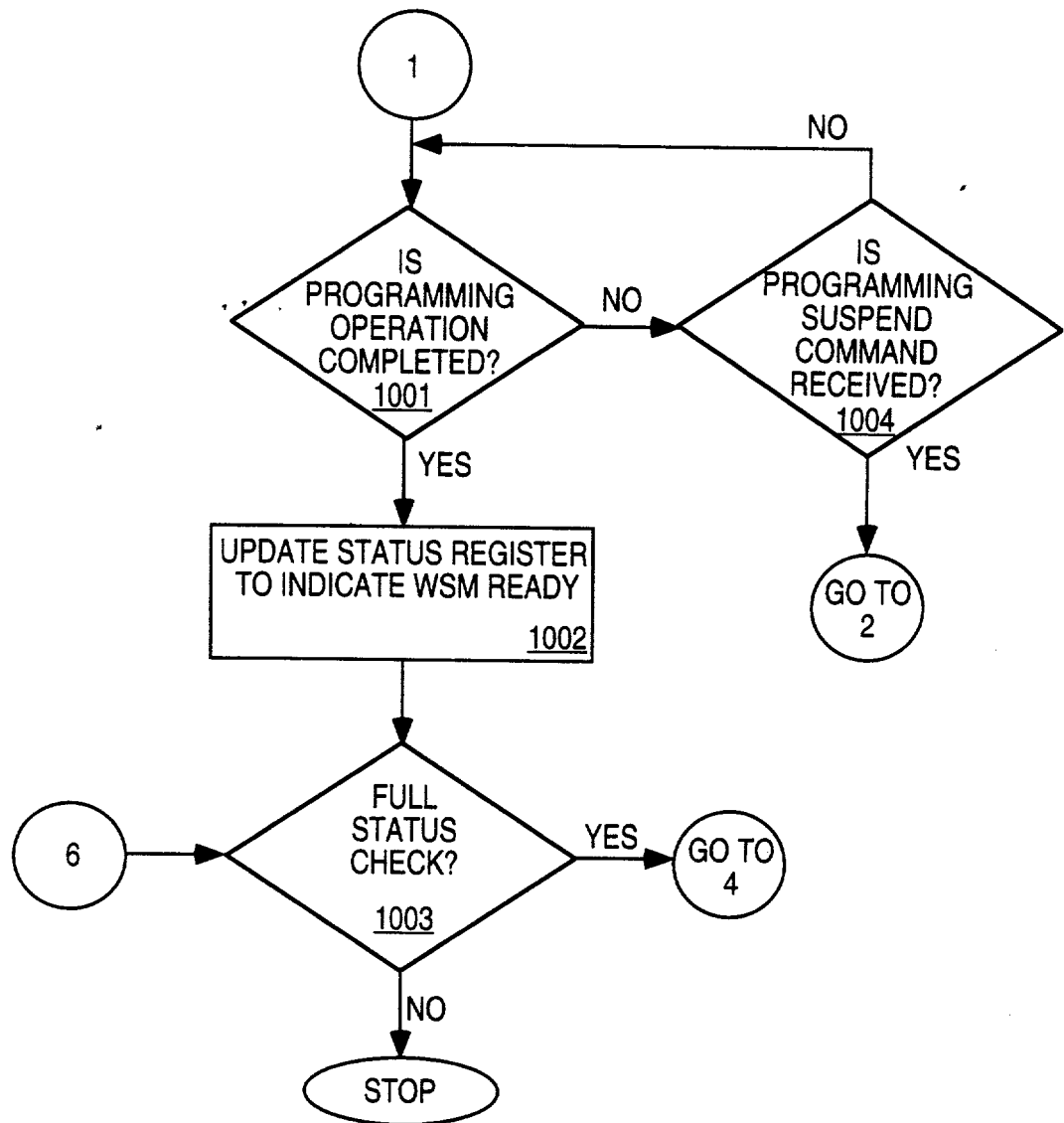


FIG. 10

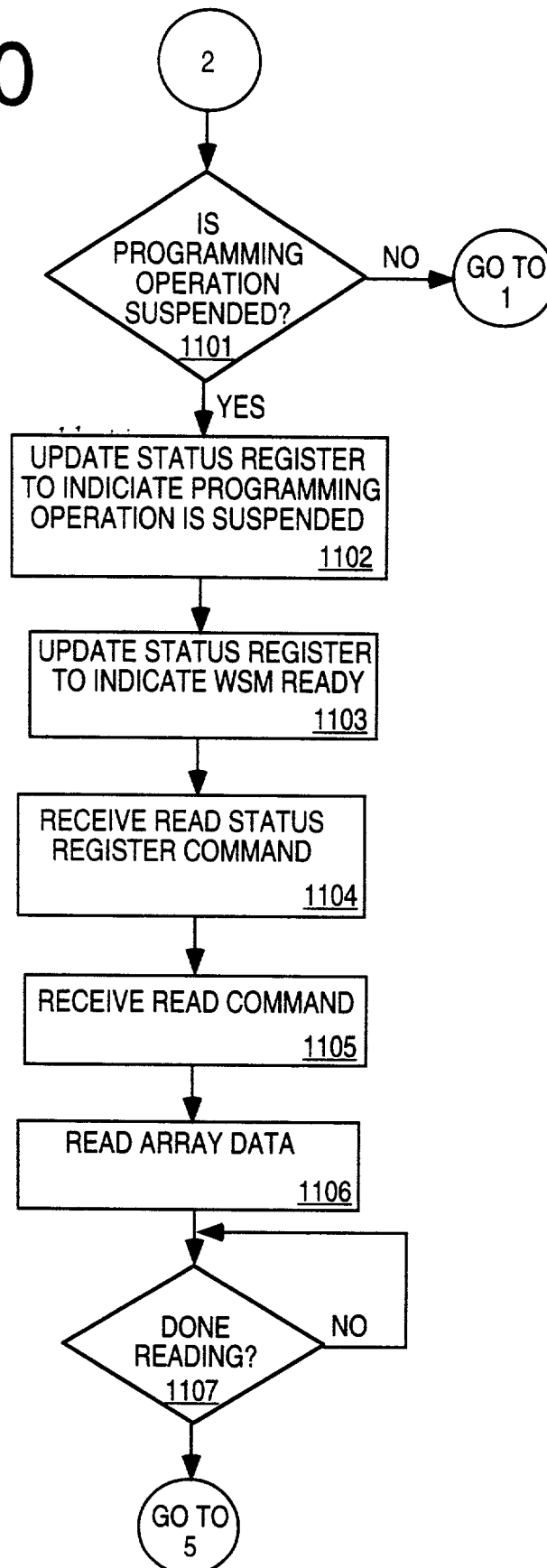


FIG. 11

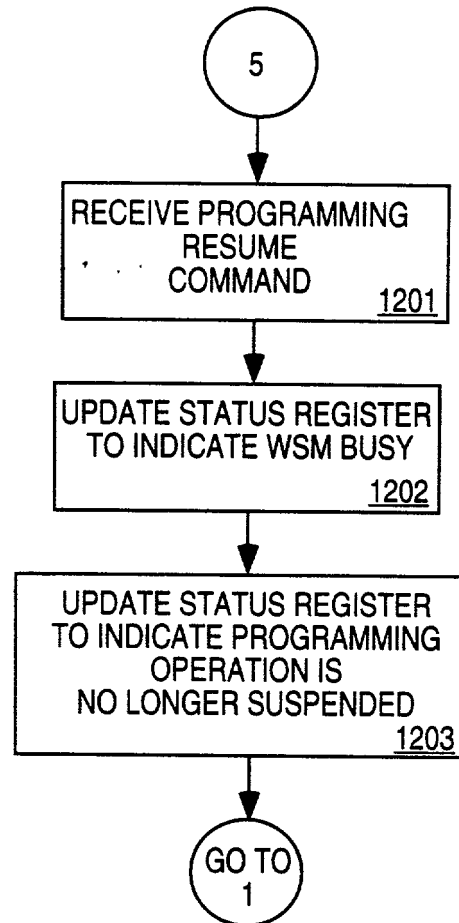


FIG. 12

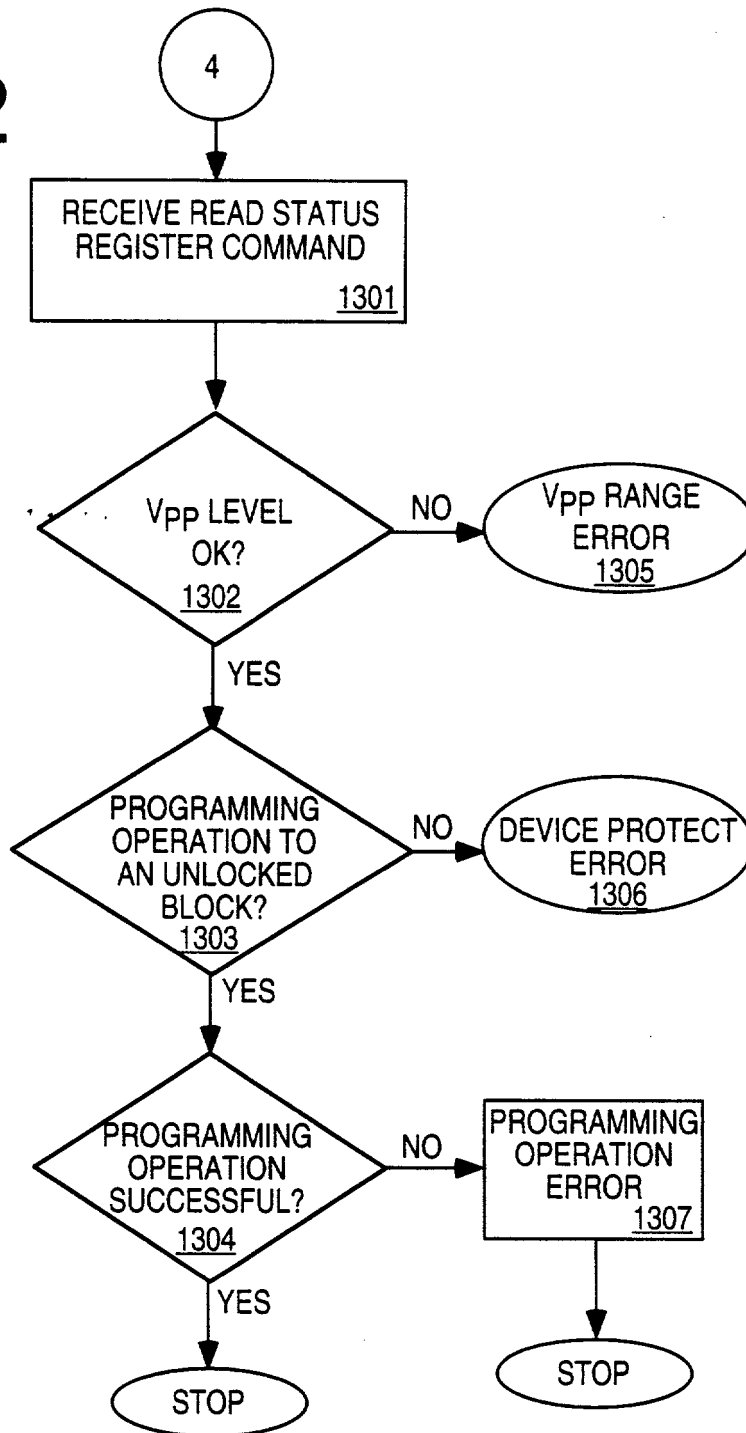


FIG. 13

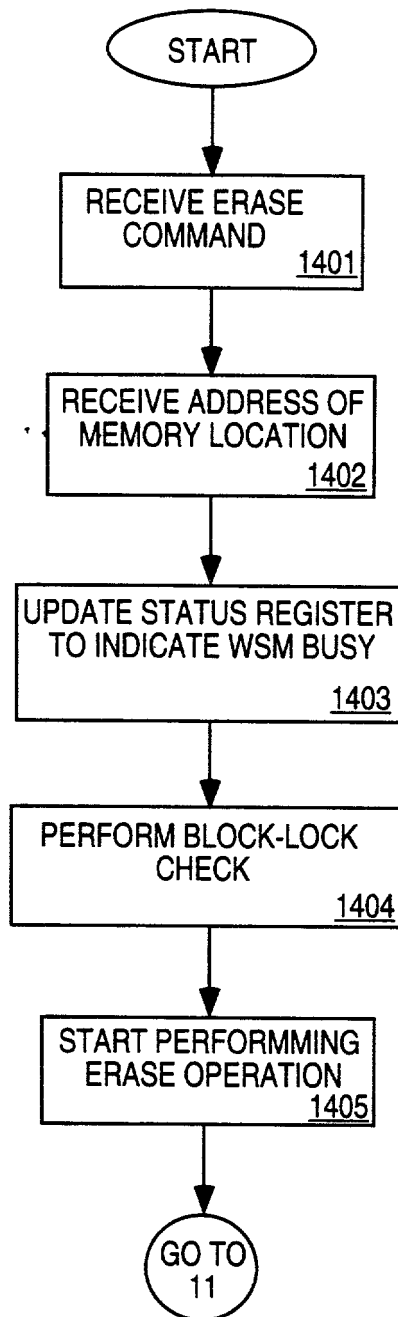


FIG. 14

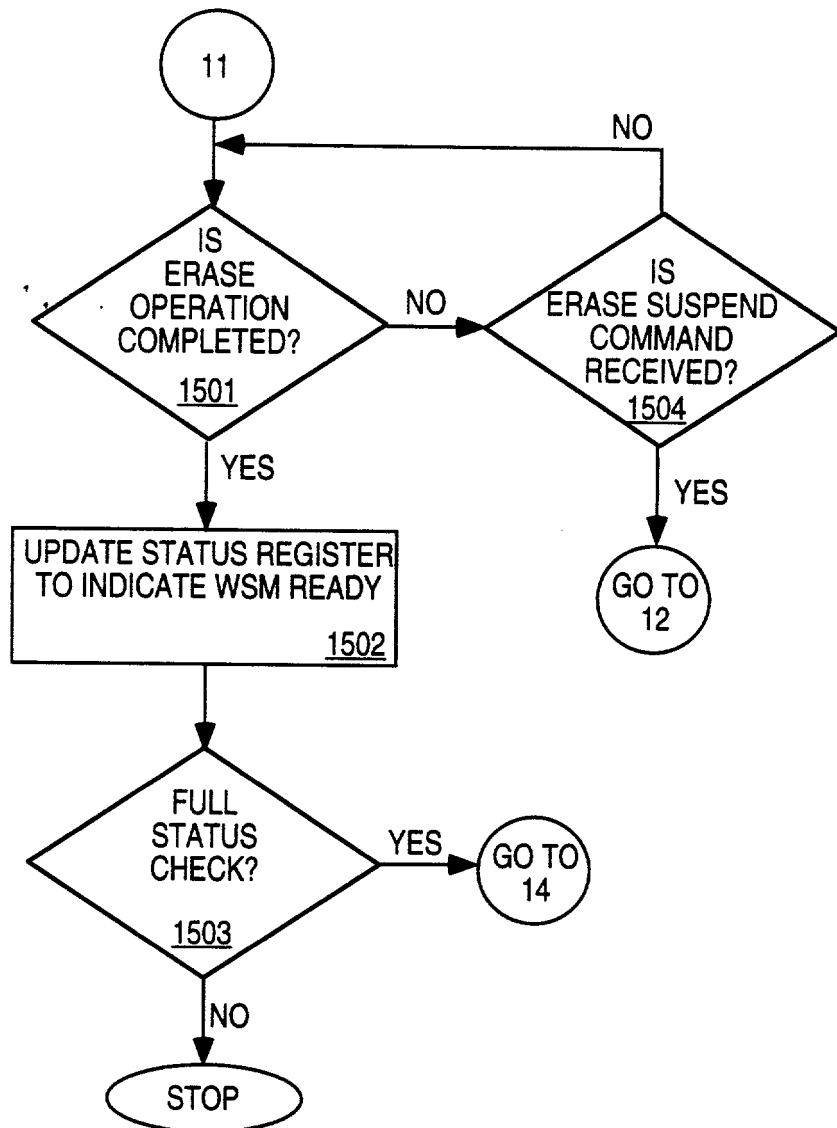


FIG. 15

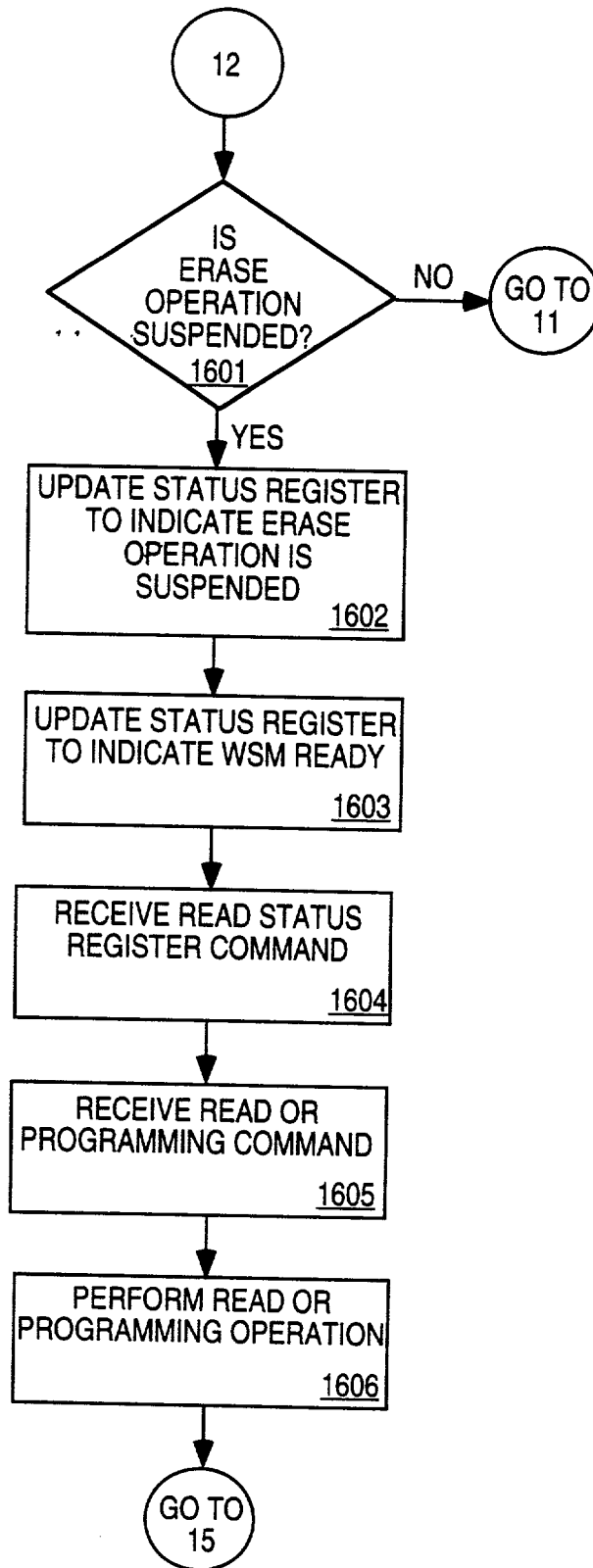


FIG. 16

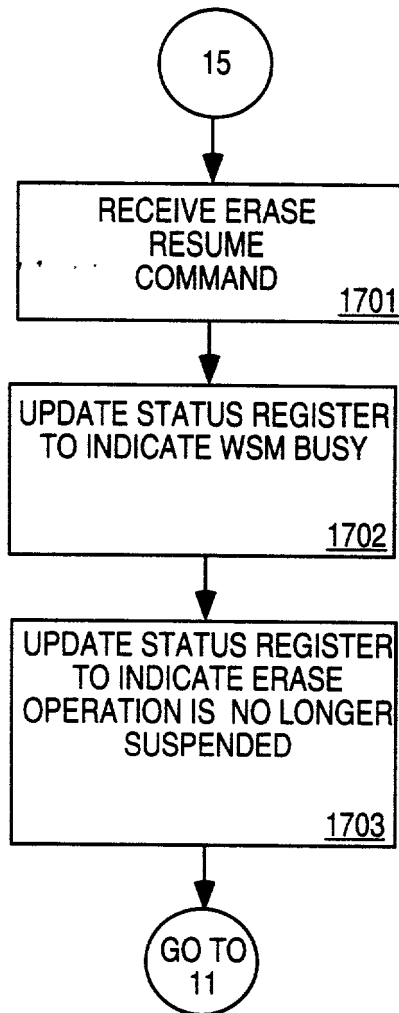


FIG. 17

